UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte MARTIN CZECH and PETER GRAF

Appeal 2007-1552
Application 09/852,123
Technology Center 3600

Decided: July 26, 2007

Before STUART S. LEVY, MAHSHID D. SAADAT and LINDA E. HORNER, *Administrative Patent Judges.*

HORNER, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF THE CASE

Appellants seek our review under 35 U.S.C. § 134 of the Examiner's rejection of claims 1-12, all the claims currently pending in the application. We have jurisdiction under 35 U.S.C. § 6(b) (2002).

SUMMARY OF DECISION

We AFFIRM.

THE INVENTION

Appellants' claimed invention is to a structure for providing electrostatic discharge (ESD) protection to an integrated semiconductor circuit (Specification 1:10-12). Claim 1, reproduced below, is representative of the subject matter on appeal.

> 1. An electrostatic discharge (ESD) protective structure that protects an integrated circuit connected between a first voltage bus with a first supply voltage (VCC) and a second voltage bus with a second supply voltage (VSS), said electrostatic discharge protective structure comprising:
>
> a plurality of laterally designed bipolar transistors each having a first load line connected to the first voltage bus and a second load line connected to the second voltage bus, wherein said first load lines are electrically parallel to one another and said second load lines are electrically parallel to one another, each of said laterally designed bipolar transistors includes a control connection to one of the voltage buses;
>
> a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally designed bipolar transistors (T1-T3).

THE REJECTIONS

The Examiner relies upon the following as evidence of unpatentability:

Avery	US 5,043,782	Aug. 27, 1991
Li	US 5,623,387	Apr. 22 1997
Smith	US 6,075,271	Jun. 13, 2000
Wong	US 6,277,689 B1	Aug. 21, 2001

The following rejections are before us for review.

1. Claim 1 stands rejected under 35 U.S.C. § 102(b) as anticipated by Avery.[1]
2. Claims 2-5 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Avery and Smith.
3. Claim 6 stands rejected under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, and Li.
4. Claims 7-12 stand rejected under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, Li, and Wong.

ISSUES

Appellants contend that Avery fails to anticipate claim 1 because Avery fails to disclose "a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally bipolar transistors (T1-T3)" (Reply Br. 3). The Examiner found that the p-doped substrate of Avery constituted "a resistor (RS) co-integrated into a semiconductor body preceding the control connection for all of the aforementioned laterally designed bipolar transistors QL and QS" (Answer 3).

The issues before us are:

1) Whether Appellants have shown that the Examiner erred in rejecting claim 1 under 35 U.S.C. § 102(b) as anticipated by Avery.

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[1] The Answer introduces this rejection as a new ground of rejection (Answer 12-13) and fails to reiterate the previous rejection of claim 1 as unpatentable over Avery in view of Wada or Ravanelli (Final Office Action 2). Accordingly, we deem the Examiner to have withdrawn the previous rejection of claim 1.

2) Whether Appellants have shown that the Examiner erred in rejecting claims 2-5 under 35 U.S.C. § 103(a) as unpatentable over Avery and Smith.

3) Whether Appellants have shown that the Examiner erred in rejecting claim 6 under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, and Li.

4) Whether Appellants have shown that the Examiner erred in rejecting claims 7-12 under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, Li, and Wong.

FINDINGS OF FACT

The relevant facts include:

1. Avery teaches an electrostatic discharge (ESD) protection device for protecting integrated circuits (Avery, col. 1, ll. 6-9).

2. The effective equivalent circuit of the protection device, shown in Fig. 7, includes a parasitic NPN transistor QS provided by the short channel length structure 16 and a plurality of parasitic NPN transistors QL provided by the plurality of longer channel length structures 18. The NPN transistor QS has its collector electrode connected to bus 20 through collector resistor RC and its emitter electrode connected to the reference line 22 through emitter resistor RE, and its base electrode connected in common with the base electrode of NPN transistor QL via the common substrate 12 and through emitter-base shunt resistance RS to the reference line 22 (Avery, col. 6, ll. 37-53).

3. The base and emitter regions/gates are effectively short-circuited with each other and connected to reference line 22 via the semiconductor substrate 12 and electrode 24 (Avery, Fig. 4, and col. 5, ll. 37-41).

4. The lightly-doped substrate 12 provides the emitter-base shunt resistance RS (Avery, Fig.7, col. 5, ll. 42-44, and col. 6, ll. 44-46).

5. Avery further teaches the ESD structure includes at least one emitter zone 42 and at least one collector zone 44 of a first conduction type N, at least one base zone 58 of a second conduction type P, and a well-shaped region 56 of the first conduction type N (Avery, Fig. 4, col. 5, ll. 10-15 and col. 5, ll. 47-51).

6. Smith teaches a semiconductor device having a stacked-gate buffer that inhibits parasitic bipolar effects during electrostatic discharge or electrical overstress (Smith, col. 1, ll. 6-10).

7. Smith teaches a well-shaped region 80 which inhibits the initiation of bipolar action by creating a blocking of, or a long path for, avalanche generated holes needed in order to forward bias the parasitic bipolar transistor formed by the transistors 95 and 105 (Smith, Fig. 7 and col. 8, ll. 42-50).

8. The term "track resistor" does not have a customary meaning in the art.

9. Appellants point to page 4, lines 8-9 [*sic*, lines 7-8] and page 7, lines 16-19 of the Specification for a discussion of the claimed single track resistor (Appeal Br. 5). The cited passages state (1) "[a] single track resistor is co-integrated into the semiconductor body and precedes every control connection of the bipolar transistors," and (2) "the base connections B of the bipolar transistors

T1-T3 are short-circuited with one another and are coupled, via a track resistor RB to the reference voltage VSS and thus the emitter connections E."

10. Furthermore, the Specification discloses that the "track resistor is created by a deep implantation region or diffusion region inserted in the semiconductor body" using, for example, a "conventional trench etching process and filling [it] up with doped or *undoped* polysilicon or with a dielectric" (Specification 4:10-11 and 5:8-10) (emphasis added).

11. The Specification further states, "It is contemplated that the well-shaped regions *may not be doped*, or may include a dielectric" (Specification 5:3-4) (emphasis added).

12. Accordingly, we find, *sua sponte*, that the Specification supports a broad interpretation of the term "track resistor." More specifically, we find that the track resistor is a region within the semiconductor body (*i.e.,* substrate) which is either (1) doped, (2) undoped, or (3) a dielectric.

13. If the region is undoped, it is the parasitic resistance of the substrate which acts as the track resistor.

PRINCIPLES OF LAW

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the

reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient." *In re Robertson*, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted) (internal quotation marks omitted).

"Section 103 forbids issuance of a patent when 'the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.'" *KSR Int'l Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1734, 82 USPQ2d 1385, 1391 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18, 148 USPQ 459, 467 (1966). *See also KSR*, 127 S.Ct. at 1734, 82 USPQ2d at 1391 ("While the sequence of these questions might be reordered in any particular case, the [*Graham*] factors continue to define the inquiry that controls.") The Court in *Graham* further noted that evidence of secondary considerations "might be utilized to give light to the circumstances surrounding the origin of the subject matter sought to be patented." 383 U.S. at 18, 148 USPQ at 467.

In *KSR*, the Supreme Court emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *id.* at 1739, 82 USPQ2d at 1395, and discussed circumstances in which a patent might be

determined to be obvious. In particular, the Supreme Court emphasized that "the principles laid down in *Graham* reaffirmed the 'functional approach' of *Hotchkiss*, 11 How. 248." *KSR,* 127 S.Ct. at 1739, 82 USPQ2d at 1395 (citing *Graham v. John Deere Co.*, 383 U.S. 1, 12 (1966) (emphasis added)), and reaffirmed principles based on its precedent that "[t]he combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *Id.* The Court explained:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, §103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

Id. at 1740, 82 USPQ2d at 1396. The operative question in this "functional approach" is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id.*

The Supreme Court stated that "[f]ollowing these principles may be more difficult in other cases than it is here because the claimed subject matter may involve more than the simple substitution of one known element for another or the mere application of a known technique to a piece of prior art ready for the improvement." *Id.* The Court explained, "[o]ften, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known

to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue." *Id.* at 1740-41, 82 USPQ2d at 1396. The Court noted that "[t]o facilitate review, this analysis should be made explicit." *Id.*, citing *In re Kahn*, 441 F.3d 977, 988, 78 USPQ2d 1329, 1336 (Fed. Cir. 2006) ("[R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness"). However, "the analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, for a court can take account of the inferences and creative steps that a person of ordinary skill in the art would employ." *Id.*

ANALYSIS

Rejection of claim 1 under 35 U.S.C. § 102(b) as anticipated by Avery

Appellants contend that Avery fails to disclose "a single track resistor (RB) co-integrated into a semiconductor body, wherein said single track resistor precedes every control connection (B) of said laterally bipolar transistors (T1-T3)" because (1) the Examiner's reliance on the equivalent circuit illustrated FIG. 7 is improper because "an equivalent circuit is simply a mathematic mechanism for representing an electrical network" and "not the actual structure of the circuit," and (2) "[a]s shown in FIG. 1, the gate electrode 34 runs to only the shorter length

channel structure 16, and not to the longer channel length structures 18a-18d" (Reply Br. 3). We do not find Appellants' arguments persuasive.

With regard to Appellants' first argument, we note that the only reference in Appellants' drawings to the track resistor RB is in regard to the equivalent structure of FIG. 2. However, similar to Avery's Figure 7, FIG. 2 of Appellants' Specification is merely an equivalent circuit and does not illustrate the actual structure of a circuit. Therefore, using Appellants' reasoning, there is no support in the Specification for a single track resistor as claimed. Clearly, Appellants would agree that such reasoning is unfounded.

With regard to Appellants' second argument, we note that claim 1 does not require a "gate electrode" which runs to each gate region, but rather only requires a control connection connected to one of the voltage buses via a single track resistor. Avery discloses the base and emitter regions/gates are short-circuited with each other and connected to reference line 22 via the semiconductor substrate 12 and electrode 24 (Finding of Fact 3). Furthermore, we find that the lightly-doped substrate 12 of Avery meets the claimed "track resistor" giving that claim term its broadest reasonable interpretation in view of the Specification (Findings of Fact 8-13). As such, we sustain the Examiner's rejection of claim 1 as anticipated by Avery.

Rejection of claims 2-5 under 35 U.S.C. § 103(a) as unpatentable over Avery and Smith

In rejecting claim 2, the Examiner found that "the use of a deeper doped region or well to significantly increase the path length that avalanche generated charge carriers have to travel as a means to increase the collector-to-emitter voltage in bipolar transistor dynamics is a method well known in the art, as witnessed by Smith" (Answer 4). Further, the Examiner held that it would have been obvious to modify the ESD structure of Avery to include a deeper doped region or well to significantly increase the path length charge carriers have to travel as illustrated in Smith (Answer 5).

Appellants contend that "Smith has nothing to do with ESD protective devices" and although "Smith illustrates a block labeled ESD circuit 15, Smith clearly states that this ESD circuit 15 is not disclosed within the specification or figures of the patent" (Reply Br. 4) (emphasis omitted). Therefore, Appellants conclude that one skilled in the art of "ESD devices would not combine Smith with Avery since Smith does not relate to ESD devices" (Reply Br. 5). We disagree.

Clearly, Smith is *related* to ESD devices as Smith explicitly discloses that it is related to "a semiconductor device having a stacked-gate that inhibits parasitic bipolar effects during *electrostatic discharge"* (emphasis added) (Finding of Fact 6). Furthermore, Appellants' contention that the deeper doped region 80 of Smith is associated with the stacked buffer and not the ESD structure is not germane to the rejection of claim 2 in as much as the Examiner cites Smith for its

teaching of deep well regions to increase path length as a means to increase the collector-to-emitter voltage in bipolar transistor dynamics, not a specific ESD protective structure. As such, we find Appellants' contention that one skilled in the art would not combine the teachings of Avery and Smith unpersuasive. As such, we sustain the Examiner's rejection of claims 2-5 as unpatentable over Avery and Smith.

Rejection of claim 6 under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, and Li

Appellants contend that claim 6 stands or falls with claims 2-5 (Reply Br. 5). As such, we sustain the Examiner rejection of claim 6 as unpatentable over Avery, Smith, and Li for those reasons presented, *supra*, with respect to claims 2-5.

Rejection of claims 7-12 under 35 U.S.C. § 103(a) as unpatentable over Avery, Smith, Li, and Wong

Appellants contend that claims 7-12 stand or fall with claim 6 (Reply Br. 6). As such, we sustain the Examiner's rejection of claims 7-12 as unpatentable over Avery, Smith, Li, and Wong for those reasons presented *supra*, with respect to claim 6.

CONCLUSION

We conclude that Appellants have not shown that the Examiner erred in rejecting claim 1 as anticipated by Avery, claims 2-5 as unpatentable over Avery and Smith, claim 6 as unpatentable over Avery, Smith, and Li, and claims 7-12 as unpatentable over Avery, Smith, Li, and Wong.

DECISION AND ORDER

The Examiner's decision under 35 U.S.C. § 102(b) to reject claim 1 as anticipated by Avery is affirmed. The Examiner's decision under 35 U.S.C. § 103(a) to reject claims 2-5 as unpatentable over Avery and Smith, claim 6 as unpatentable over Avery, Smith, and Li, and claims 7-12 as unpatentable over Avery, Smith, Li, and Wong is affirmed.

AFFIRMED

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O'SHEA, GETZ & KOSAKOWSKI, P.C.
1500 MAIN ST.
SUITE 912
SPRINGFIELD MA 01115